

**UNITED STATES DISTRICT COURT  
FOR THE WESTERN DISTRICT OF TEXAS  
WACO DIVISION**

ACQIS LLC,

Plaintiff,

v.

HON HAI PRECISION INDUSTRY CO.,  
LTD.,

Defendant.

Case No. 6:23-cv-264-ADA

JURY TRIAL DEMANDED

  
PUBLIC VERSION

**DEFENDANT HON HAI PRECISION  
INDUSTRY CO., LTD'S CLAIM CONSTRUCTION BRIEF**

## **TABLE OF CONTENTS**

|      |   |    |
|------|---|----|
| I.   | INTRODUCTION.....   | 1  |
| II.  | BACKGROUND.....   | 1  |
|      | A.    The Asserted Patents.....   | 1  |
|      | B.    The Relevant Technology .....   | 2  |
|      | C.    Litigation History .....  | 4  |
| III. | DISPUTED CLAIM TERMS .....  | 7  |
|      | A.    “Peripheral Component Interconnect (PCI) bus transaction” /<br>“PCI bus transaction”.....   | 7  |
|      | 1.    The Federal Circuit’s Construction Controls.....  | 7  |
|      | 2.    Plaintiff’s Proposal of “Backwards Compatibility” is<br>Contrary To, and Not a Clarification of, the<br>Federal Circuit’s Construction..... | 9  |
|      | 3.    Plaintiff’s Proposal of “Backwards Compatibility” is<br>Contrary to the Intrinsic Record. ....  | 10 |
|      | 4.    Plaintiff’s Proposal of “Backwards Compatibility”<br>Creates Ambiguity and Invites Jury Confusion.....                                      | 12 |
|      | B.    “USB” or “Universal Serial Bus” .....   | 14 |
|      | 1.    At the Time of the Invention “USB” Meant USB 2.0<br>or Earlier. ....  | 14 |
|      | 2.    Plaintiff’s “Plain and Ordinary Meaning” Invites<br>Jury Confusion.....   | 15 |
| IV.  | CONCLUSION .....  | 17 |

## **TABLE OF AUTHORITIES**

|   | <b>Page(s)</b> |
|---|----------------|
| <b>Cases</b>  |                |
| <i>ACQIS LLC v. Asustek Computer Inc.</i> ,<br>No. 20-cv-966-ADA, Dkt. No. 144 (W.D. Tex. Dec. 28, 2022) .....          | 8              |
| <i>ACQIS LLC v. Asustek Computer, Inc.</i> ,<br>No. 20-cv-966-ADA, Dkt. No. 52 (W.D. Tex. Nov. 17, 2021) .....          | 6              |
| <i>ACQIS LLC v. Samsung Electronics Co., Ltd.</i> ,<br>No. 20-cv-295-JRG, Dkt. No. 71 (E.D. Tex. Aug. 3, 2021) .....    | 15             |
| <i>ACQIS LLC v. Samsung Electronics Co., Ltd.</i> ,<br>No. 20-cv-295-JRG, Dkt. No. 92 (E.D. Tex. Sept. 26, 2021) .....  | 7              |
| <i>ACQIS, LLC v. EMC Corp.</i> ,<br>No. 21-1772, Dkt. No. 30 (Fed. Cir. Nov. 19, 2021) .....                            | 5, 9, 13       |
| <i>ACQIS, LLC v. EMC Corp.</i> ,<br>No. 13-cv-639-LED, Dkt. No. 46 (E.D. Tex. Apr. 13, 2015) .....                      | 6              |
| <i>ACQIS, LLC v. EMC Corp.</i> ,<br>No. 14-cv-13560-ADB, 2021 WL 1088207 (D. Mass. Feb. 19, 2021) .....                 | <i>passim</i>  |
| <i>ACQIS, LLC v. EMC Corp.</i> ,<br>No. 2021-1772, 2022 WL 1562847 (Fed. Cir. May 18, 2022) .....                       | <i>passim</i>  |
| <i>Amgen Inc. v. Sanofi</i> ,<br>598 U.S. 594 (2023) .....  | 12, 13, 16     |
| <i>Ariad Pharms., Inc. v. Eli Lilly &amp; Co.</i> ,<br>598 F.3d 1336 (Fed. Cir. 2010) ( <i>en banc</i> ) .....          | 13, 16         |
| <i>Aylus Networks, Inc. v. Apple Inc.</i> ,<br>856 F.3d 1353 (Fed. Cir. 2017) .....                                     | 12             |
| <i>CommScope Techs. LLC v. Dali Wireless Inc.</i> ,<br>10 F.4th 1289 (Fed. Cir. 2021) .....                             | 12             |
| <i>EMC Corp. v. ACQIS LLC</i> ,<br>IPR2014-01462, Paper 30 (PTAB June 11, 2015) .....                                   | 4, 5, 12       |
| <i>EMC Corp. v. ACQIS LLC</i> ,<br>IPR2014-01462, Paper 60 (PTAB Jan. 5, 2016) .....                                    | 4, 5, 11       |
| <i>Eolas Techs., Inc. v. Adobe Sys., Inc.</i> ,<br>No. 09-cv-446-LED, 2011 WL 11070303 (E.D. Tex. Sept. 23, 2011) ..... | 7              |

|   |        |
|---|--------|
| <i>Extreme Networks, Inc. v. Enterasys Networks, Inc.</i> ,<br>No. 07-cv-229-BBC, 2007 WL 5601497 (W.D. Wis. Nov. 21, 2007) .....         | 17     |
| <i>Fundamental Innovation Sys. Int’l LLC v. Samsung Elecs. Co.</i> ,<br>No. 17-cv-145-JRG, 2018 WL 647734 (E.D. Tex. Jan. 31, 2018) ..... | 15     |
| <i>Key Pharms. v. Hercon Lab’ys Corp.</i> ,<br>161 F.3d 709 (Fed. Cir. 1998) .....  | 7      |
| <i>Kopykake Enterprises, Inc. v. Lucks Co.</i> ,<br>264 F.3d 1377 (Fed. Cir. 2001) .....  | 17     |
| <i>Kumar v. Ovonic Battery Co.</i> ,<br>351 F.3d 1364 (Fed. Cir. 2003) .....  | 10     |
| <i>Luminara Worldwide, LLC v. Liown Elecs. Co.</i> ,<br>814 F.3d 1343 (Fed. Cir. 2016) .....  | 11, 15 |
| <i>Massachusetts Inst. of Tech. &amp; Elecs. For Imaging, Inc. v. Abacus Software</i> ,<br>462 F.3d 1344 (Fed. Cir. 2006) .....           | 15     |
| <i>O2 Micro Int’l Ltd. v. Beyond Innovation Tech. Co.</i> ,<br>521 F.3d 1351 (Fed. Cir. 2008) .....                                       | 15     |
| <i>Ottah v. Fiat Chrysler</i> ,<br>884 F.3d 1135 (Fed. Cir. 2018) .....   | 9      |
| <i>PC Connector Sols. LLC v. SmartDisk Corp.</i> ,<br>406 F.3d 1359 (Fed. Cir. 2005) .....  | 15     |
| <i>Phillips v. AWH Corp.</i> ,<br>415 F.3d 1303 (Fed. Cir. 2005) ( <i>en banc</i> ) .....   | 11, 14 |
| <i>In Re Rambus Inc.</i> ,<br>694 F.3d 42 (Fed. Cir. 2012) .....  | 7      |
| <i>SightSound Techs., LLC v. Apple Inc.</i> ,<br>809 F.3d 1307 (Fed. Cir. 2015) .....   | 8      |
| <i>SitePro, Inc. v. Waterbridge Resources LLC</i> ,<br>No. 23-cv-115-ADA-DTG, 2024 WL 760923 (W.D. Tex. Feb. 23, 2024) .....              | 15     |
| <i>Source Vagabond Sys. Ltd. v. Hydrapak, Inc.</i> ,<br>753 F.3d 1291 (Fed. Cir. 2014) .....  | 10     |
| <i>TQ Delta, LLC v. CommScope Holding Co., Inc.</i> ,<br>No. 2:21-cv-309-JRG, 2022 WL 2071073 (E.D. Tex. June 8, 2022) .....              | 8      |

## **TABLE OF EXHIBITS**

| <b><u>Exhibit No.</u></b> | <b><u>Description</u></b>  |
|---------------------------|--|
| A                         | PCI Local Bus Specification Rev. 2.2 (Dec. 18, 1998)   |
| B                         | <i>EMC Corp. v. ACQIS LLC</i> , IPR2014-01462, Paper 30 (Patent Owner’s Resp.) (PTAB June 11, 2015)  |
| C                         | <i>EMC Corp. v. ACQIS LLC</i> , IPR2014-01462, Paper No. 60 (Hearing Tr. Dec. 8, 2015) (PTAB Jan. 5, 2016)   |
| D                         | <i>EMC Corp. v. ACQIS LLC</i> , IPR2014-01462, Dkt. Nos. 1028–29 (Aug. 27–28, 2015 Dep. Tr. of Volker Lindenstruth Vols. I and II) (PTAB Sept. 10, 2015) |
| E                         | <i>ACQIS, LLC v. EMC Corp.</i> , No. 21-1772, Dkt. No. 23 (Corrected Opening Brief) (Fed. Cir. Aug. 16, 2021)  |
| F                         | Adam Wilen <i>et al.</i> , <i>Introduction to PCI Express: A Hardware and Software Developer’s Guide</i> (Intel Press 2003)                              |
| G                         | Universal Serial Bus Specification Revision 2.0 (Apr. 27, 2000)  |
| H                         | <i>ACQIS LLC v. Samsung Electronics Co., Ltd.</i> , No. 2:20-cv-295-JRG, Dkt. No. 71 (Aug. 3, 2021)  |
| I                         | <i>ACQIS LLC v. Samsung Electronics Co., Ltd.</i> , No. 2:20-cv-295-JRG (Dep. Tr. of Marc E. Levitt) (E.D. Tex. June 23, 2021)                           |
| J                         | <i>ACQIS, LLC v. EMC Corp.</i> , No. 21-1772, Dkt. No. 30 (Corrected Resp. Brief) (Fed. Cir. Nov. 19, 2021)  |
| K                         | <i>ACQIS LLC v. Hon Hai Precision Indus. Co., Ltd.</i> , No. 6:23-cv-264-ADA, ACQIS’ Amended Prelim. Infringement Contentions (Jan. 26, 2024)            |

Plaintiff ACQIS LLC (“ACQIS”) asserts five patents in this action: U.S. Patent Nos. 9,703,750 (“the ’750 Patent”); 8,977,797 (“the ’797 Patent”), 9,529,769 (“the ’769 Patent”), RE45,140 (“the RE140 Patent”); and RE44,654 (“the RE654 Patent”). Defendant Hon Hai Precision Industry Co., Ltd. (“Hon Hai”) hereby submits its opening claim construction brief.

## **I. INTRODUCTION**

Hon Hai seeks construction of two terms. The first—“Peripheral Component Interconnect (PCI) bus transaction” or “PCI bus transaction”—has already been construed by the Federal Circuit. The Federal Circuit’s construction controls. ACQIS’ attempts to inject ambiguity through an unsupported construction requiring only “backwards compatibility” should be rejected. The second term at issue—“Universal Serial Bus” or “USB”—had a well-established plain and ordinary meaning at the time of the invention. ACQIS’ attempts to broaden its claims to encompass later USB versions is improper and inconsistent with fundamental claim construction principles. Accordingly, the Court should adopt Hon Hai’s proposed constructions.

## **II. BACKGROUND**

### **A. The Asserted Patents**

The Asserted Patents fall into two categories: The non-reissue patents (the ’750, ’769, and ’797 Patents) relate to “a system including a plurality of computer modules that can independently operate to provide backup capability, dual processing, and the like.” *See, e.g.,* ’797 Patent, 1:32–36. The non-reissue patents share substantially identical specifications, and claim methods of, *e.g.*, “improving peripheral data communication within a computer” using Low Voltage Differential Signal (“LVDS”) channels. *See, e.g., id.* at 41:42–43. The remaining two patents are reissues (the RE140 and RE654 Patents), with specifications directed to “a method and device for securing a personal computer or set-top box” and teachings irrelevant to the reissue claims (*see, e.g.,* RE140 Patent, 1:35–37), which instead recite “method[s] of

improving performance of a computer” using LVDS channels, similar to the non-reissue patents (*see, e.g., id.* at 22:44–45).

## **B. The Relevant Technology**

ACQIS’ patents describe a “modular” computer system, reliant on and compatible with technology well-known at the time of invention—specifically, a “computer module,” including CPU and memory, that inserts into a “console” with connections for peripheral devices, such as monitors, keyboards, and mice. *See, e.g.,* ’797 patent, 9:40–10:18, Fig. 1. According to the patents, the “invention is . . . implemented using conventional technologies” available at the time of invention, “that can be provided in the present computer system in an easy and efficient manner.” *Id.* at 7:37–40. The inventions’ purported advance over the prior art is the “advantageous[]” use of LVDS channels to interface PCI buses. *Id.* at 5:54–56.

The Asserted Patents state that “[i]nterfaces coupling two independent computer buses are well known in the art,” but, “as a result of operating by PCI protocols, the prior art interface includes a very large number of signal channels with a corresponding large number of conductive lines (and a similarly large number of pins in the connectors of the interface).” ’797 Patent, 3:13–56. The large number of pins and wires were used for parallel transactions: PCI interfaces send multiple bits of information simultaneously over the separate, dedicated wires (*i.e.*, in “parallel”). *See* Ex. A, PCI Local Bus Specification Rev. 2.2 at 7 (Dec. 18, 1998). According to the patents, these prior art interfaces were costly, “bulkier,” and “cumbersome.” ’797 Patent, at 3:56–61. To that end, the patents purport to disclose a new physical interface with faster communication speeds. *Id.* at 15:15–41.

Long before the purported inventions of the Asserted Patents, PCI bus communications were standardized and defined in the PCI Local Bus Specification to ensure compatibility across devices. *See* Ex. A, PCI Local Bus Specification Rev. 2.2 at 1. The PCI Local Bus Specification at the time of the purported inventions used “parallel” transactions for data

communication. Under the PCI Local Bus Specification, a transaction is an exchange of information that takes place in a specific sequence and manner, with the Specification setting out both the information that must be communicated, and how it is transmitted. *See id.* at 7–16.

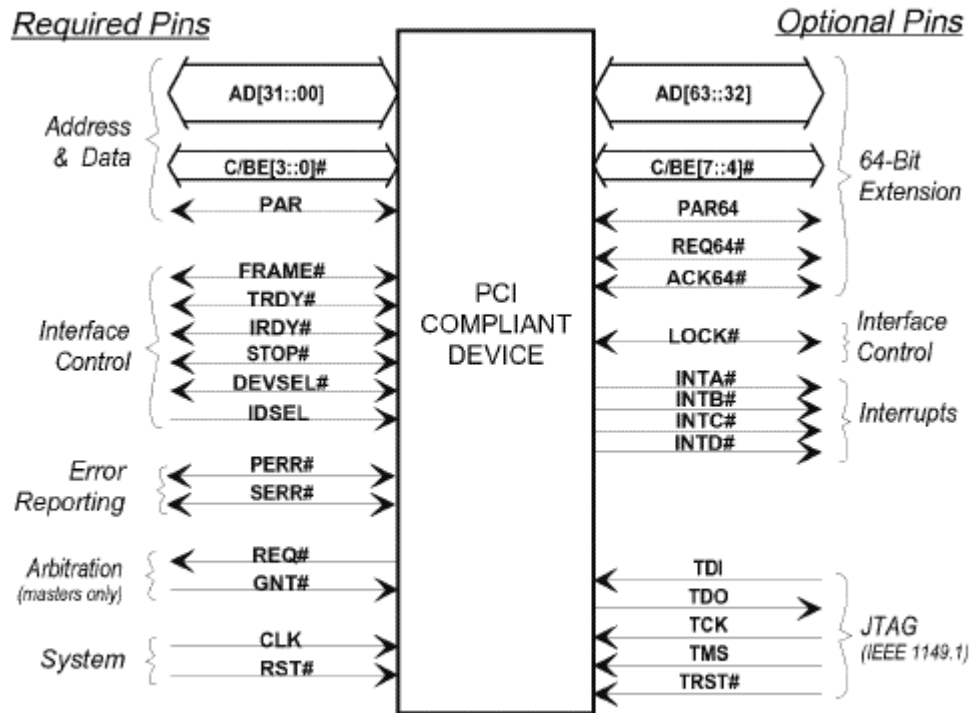


Figure 2-1: PCI Pin List

*Id.* at 7.

Specifically, a PCI bus transaction occurs in two “phases”—an “address phase followed by one or more data phases.” *Id.* at 9 (footnote omitted). During each phase, 32 bits (representing either address or data signals) are generated for parallel transmission. *Id.* A PCI bus transaction also requires control, command and byte enable, and parity signals. Control signals, such as “FRAME#,” “IRDY#,” and “TRDY#,” define the beginning and end of various PCI bus transactions. *Id.* at 10–11; *see also id.* at 47–48 (explaining that a read or write transaction “starts with an address phase which occurs when FRAME# is asserted for the first time”). These three signals control the “fundamentals of all PCI data transfers.” *Id.* at 26. Command and byte enable signals indicate what “type of transaction” has been requested. *Id.*



at 21–23; *see also id.* at 9. The PCI bus transactions require a parity signal for error detection, “to determine for each transaction” if the correct components have communicated and “if data transfers correctly between them.” *Id.* at 94. “Parity generation is not optional; it must be done by all PCI compliant devices.” *Id.*; *see also id.* at 10 (“Parity generation is required by all PCI agents.”).

The most fundamental feature of ACQIS’ purported invention is support for data conversion from parallel (*i.e.*, PCI) into serial (*i.e.*, LVDS) data formats. ’797 Patent, 17:18–58. ACQIS emphasized in related *inter partes* review (“IPR”) proceedings that, at the time of the invention, “PCI had been widely adopted,” and ACQIS sought to “develop[] a system . . . that was completely compatible with existing peripheral devices.” Ex. B, *EMC Corp. v. ACQIS LLC*, IPR2014-01462, Paper 30 at 3 (Patent Owner’s Response) (PTAB June 11, 2015). This meant that, while changing the interface to include serial LVDS channels, the invention preserved the entirety of the PCI Local Bus Specification for transactions. *Id.* at 3, 10; *see also id.* at 8 (arguing that “PCI is an industry standard,” that as a standard, PCI “ensure[s] that multiple designers can develop hardware and software and that it will all work together,” that “[e]ven minor deviations from a standard will result in incompatible hardware and software,” and, as such, ACQIS’ invention “adheres to the PCI standard”); Ex. C, *EMC Corp. v. ACQIS LLC*, IPR2014-01462, Paper 60 at 31:18–32:4 (counsel for ACQIS representing to the PTAB that “[t]he content has to be the same” because “[t]hat’s what the claims require. If you don’t do that, you have destroyed your PCI standard. You have destroyed the very purpose of this invention.”).

### **C. Litigation History**

ACQIS has litigated the Asserted Patents at length, as well as patents in the same family with overlapping claim language and intrinsic records. Importantly, the Federal Circuit has

already construed the term “PCI Bus transaction” and related terms, and several district courts have addressed the term “USB.”

Over the past decade of litigation, ACQIS has put forward contradictory interpretations of “PCI Bus transaction,” in an attempt to avoid invalidity while maintaining a plausible claim of infringement. In prior IPRs of related patents,<sup>1</sup> ACQIS argued that “[t]he proper construction for ‘Peripheral Component Interconnect (PCI) bus transaction’ is,” precisely as Hon Hai argues here, “Peripheral Component Interconnect (PCI) industry standard bus transaction,” because “[a]ny other reading of the term would render the phrase ‘PCI’ meaningless.” Ex. B, *EMC*, IPR2014-01462, Paper 30 at 17–18. Accordingly, in related district court litigation,<sup>2</sup> ACQIS initially stipulated to that same construction, only to change course at summary judgment, when it became clear that the previously agreed construction precluded infringement by devices practicing the modern PCI Express (“PCIe”) standard.<sup>3</sup> Despite ACQIS’ change of heart, the district court affirmed its claim constructions, as outlined below, and granted the defendant summary judgment of non-infringement.

| <b>Claim Term</b>   | <b>Court’s Construction</b>   |
|---|---|
| “Peripheral Component Interconnect (PCI) bus transaction” | “a transaction, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component.” |

<sup>1</sup> In IPR2014-01462, ACQIS argued against invalidation of U.S. Patent No. 8,041,873. In IPR2014-01469, ACQIS argued against invalidation of U.S. Patent No. RE42,814. ACQIS presented similar arguments in both proceedings, with a joint hearing. See Ex. C, *EMC Corp. v. ACQIS LLC*, IPR2014-01462, Paper 60 (Hearing Tr. Dec. 8, 2015) (PTAB Jan. 5, 2016).

<sup>2</sup> In *ACQIS, LLC v. EMC Corp.*, ACQIS asserted U.S. Patent Nos. 7,363,416, 7,818,487, 8,041,873, RE41,294, RE42,814, RE43,119, RE43,171, and RE44,468. *ACQIS, LLC v. EMC Corp.*, No. 14-cv-13560-ADB, 2021 WL 1088207, at \*1 (D. Mass. Feb. 19, 2021) (“*EMC I*”).

<sup>3</sup> The modern standard, PCIe, is profoundly different from PCI. As explained by its inventor, Ajay Bhatt, PCIe was a completely new protocol, created “from the ground up,” and its name was “not meant to indicate any hardware or protocol compatibility with the PCI Local Bus Specification.” Ex. J, *ACQIS, LLC v. EMC Corp.*, No. 21-1772, Dkt. No. 30 (Corrected Resp. Brief) at 10 (Fed. Cir. Nov. 19, 2021). PCIe is “a new, fully serial, point-to-point interconnect” system that is “not compatible with the PCI Local Bus Specification transaction protocol.” *Id.*; see also Ex. F, Adam Wilen *et al.*, *Introduction to PCI Express: A Hardware and Software Developer’s Guide* (Intel Press 2003).

| Claim Term   | Court's Construction   |
|--|--|
| "Encoded . . . serial bit stream of Peripheral Component Interconnect (PCI) bus transaction and related terms" | "a PCI bus transaction that has been serialized from a parallel form"                |
| "communicating . . . PCI bus transaction."   | "communicating a PCI bus transaction, including all address, data, and control bits" |

See *ACQIS, LLC v. EMC Corp.*, No. 13-cv-639-LED, Dkt. No. 46 (Mem. Opinion and Order on Claim Construction) at 32 (E.D. Tex. Apr. 13, 2015); see also *EMC I*, 2021 WL 1088207 at \*2, \*3–6.

ACQIS appealed the district court's claim construction and judgment of non-infringement to the Federal Circuit, arguing that the district court erred in concluding that "PCI bus transaction" requires a transaction in accordance with the PCI Local Bus Specification. See Ex. E, *ACQIS, LLC v. EMC Corp.*, No. 21-1772, Dkt. No. 23 (Corrected Opening Brief) at 4 (Fed. Cir. Aug. 16, 2021). According to ACQIS, only part of the industry standard PCI bus transaction was required, with an emphasis on purported "backwards compatibility." *Id.* at 11–13, 44–53. The Federal Circuit found this unpersuasive. The court "specifically adopt[ed] the district court's constructions of the terms 'Peripheral Component Interconnect (PCI) bus transaction,' 'encoded . . . serial bit stream of Peripheral Component Interconnect (PCI) bus transaction,' 'communicating . . . PCI bus transaction,' and related terms," affirming the district court's summary judgment of no infringement by PCIe. *ACQIS, LLC v. EMC Corp.*, No. 2021-1772, 2022 WL 1562847, at \*1 (Fed. Cir. May 18, 2022) ("*EMC IP*"); see also *id.* at \*1 n.1 ("The asserted claims use slight variations on these terms. . . . We believe that the district court was correct in treating these related terms similarly.").

ACQIS has also litigated the term "USB" before. This Court has given the term its plain and ordinary meaning. *ACQIS LLC v. Asustek Computer, Inc.*, No. 20-cv-966-ADA, Dkt. No. 52 at 9 (W.D. Tex. Nov. 17, 2021). The Eastern District of Texas has also given the term its plain and ordinary meaning, but at the time of invention: "the protocols defined in the Universal Serial Bus Specification Revision 2.0 and the prior versions of this standard."

*ACQIS LLC v. Samsung Electronics Co., LTD.*, No. 20-cv-295-JRG, Dkt. No. 92 at 29–33 (E.D. Tex. Sept. 26, 2021).

### III. DISPUTED CLAIM TERMS

#### A. “Peripheral Component Interconnect (PCI) bus transaction” / “PCI bus transaction”

| Claim Term  | Defendant’s Construction   | Plaintiff’s Construction  |
|---|--|---|
| “Peripheral Component Interconnect (PCI) bus transaction”/ “PCI bus transaction”<br><br>’797 Patent, claims 36, 38<br>RE140 patent, claims 16, 30<br>RE654 patent, claim 21 | “a transaction, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component” | “A transaction, in accordance <b>or backwards compatible with</b> the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component” |

The Federal Circuit has already construed “Peripheral Component Interconnect (PCI) bus transaction,” to mean, as Hon Hai proposes, “a transaction, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component.” *See EMC II*, 2022 WL 1562847, at \*2. ACQIS’ attempt to re-litigate this issue, and resurrect its preferred “backwards compatibility” construction should be rejected as contrary to the ruling of the Federal Circuit, as well as the intrinsic record.

#### 1. The Federal Circuit’s Construction Controls.

The claim construction adopted by the Federal Circuit is binding on district courts. *See, e.g., Key Pharms. v. Hercon Lab’ys Corp.*, 161 F.3d 709, 716 (Fed. Cir. 1998) (recognizing “the national *stare decisis* effect that this court’s decisions on claim construction have”); *Eolas Techs., Inc. v. Adobe Sys., Inc.*, No. 09-cv-446, 2011 WL 11070303, at \*2 (E.D. Tex. Sept. 23, 2011) (same). It is well-established that the “same claim term in the same patent or related patents carries the same construed meaning.” *In Re Rambus Inc.*, 694 F.3d 42, 48 (Fed. Cir. 2012).

Here, the Federal Circuit “specifically adopt[ed] the district court’s constructions of the terms ‘Peripheral Component Interconnect (PCI) bus transaction,’ ‘encoded . . . serial bit

stream of Peripheral Component Interconnect (PCI) bus transaction,’ . . . and related terms.” *EMC II*, 2022 WL 1562847, at \*1; *see also id.* at \*1 n.1. The term “PCI Bus transaction” therefore requires “a transaction in accordance with the industry standard PCI Local Bus Specification,” and an “encoded . . . serial bit stream of Peripheral Component Interconnect (PCI) bus transaction” requires “a PCI bus transaction that has been serialized from a parallel form.” *Id.* at \*1; *see also EMC I*, 2021 WL 1088207, at \*2, \*4–6. The Federal Circuit further affirmed that the recited “PCI Bus transaction” does not extend to PCIe, because a “PCI Bus transaction” requires data transfer “in accordance with” the PCI bus standard. *EMC II*, 2022 WL 1562847, at \*1; *see also EMC I*, 2021 WL 1088207, at \*4.

The Federal Circuit’s construction applies to the Asserted Patents. The Asserted Patents are closely related to the patents at issue before the Federal Circuit, having (1) the same patent families; (2) the same, sole inventor; (3) the same subject matter; (4) many shared claim limitations; and moreover, (5) all the patents claim priority to the same provisional application. “Where multiple patents ‘derive from the same parent application and share many common terms, we must interpret the claims consistently across all asserted patents.’” *SightSound Techs., LLC v. Apple Inc.*, 809 F.3d 1307, 1316 (Fed. Cir. 2015) (citations omitted); *see also TQ Delta, LLC v. CommScope Holding Co., Inc.*, No. 21-cv-309-JRG, 2022 WL 2071073, at \*59 (E.D. Tex. June 8, 2022) (similar). Thus, the Asserted Patents are subject to the same claim construction as adopted by the Federal Circuit.

Indeed, this Court has already found as much, extending the Federal Circuit’s constructions in *EMC* to the patents and claim terms at issue here. *See, e.g., ACQIS LLC v. Asustek Computer Inc.*, No. 20-cv-966-ADA, Dkt. No. 144 at 2 (Order on Federal Circuit claim constructions) (W.D. Tex. Dec. 28, 2022) (holding the Federal Circuit’s construction applies to “encoding” PCI terms where, as here, the claims recite “encoded,” “serial,” and “PCI bus

transaction”). ACQIS’ collateral attack on the Federal Circuit’s claim construction should be rejected.

**2. Plaintiff’s Proposal of “Backwards Compatibility” is Contrary To, and Not a Clarification of, the Federal Circuit’s Construction.**

By adding “backwards compatibility,” ACQIS attempts to impermissibly broaden the Federal Circuit’s construction. The Federal Circuit required full compliance with the PCI Local Bus Specification. *EMC II*, 2022 WL 1562847, at \*1; *see also EMC I*, 2021 WL 1088207, at \*4. In so doing, the Federal Circuit rejected, as the Massachusetts district court had before, ACQIS’ attempts to broaden its claims’ plain meaning, to capture later-developed, profoundly different PCIe technology. *EMC II*, 2022 WL 1562847, at \*1; *see also EMC I*, 2021 WL 1088207, at \*4 (“All of ACQIS’ arguments are attempts to skirt the claim construction set forth by Judge Davis and this Court.”). Before the Federal Circuit, ACQIS emphasized that its purported invention was “replacing parallel buses with serial interface channels—specifically, [LVDS] channels—that maintained backwards compatibility” with the PCI Local Bus Specification. Ex. E, *EMC II*, No. 21-1772, Dkt. No. 23 at 12. It argued that an incomplete PCI transaction was sufficient, having only “transaction layer data.” *Id.* at 35–36, 49, 53–55. The Federal Circuit heard and rejected ACQIS’ “backwards compatibility” argument, instead “specifically adopt[ing]” the district court’s requirement that there be a complete PCI transaction, “in accordance with” the entire PCI Local Bus Specification. *EMC II*, 2022 WL 1562847, at \*1; *see also EMC I*, 2021 WL 1088207, at \*4.

Whatever ACQIS means by “backwards compatible,” it cannot vitiate the claim requirement for a complete PCI Local Bus Specification transaction, including all address, data, control, command and byte enable, and parity signals, as recited in the PCI standard. This claim construction “issue was finally decided and is not subject to collateral review.” *Ottah v. Fiat Chrysler*, 884 F.3d 1135, 1139 (Fed. Cir. 2018). As the Federal Circuit has held—and ACQIS previously argued—“PCI Bus transaction” requires “a transaction in accordance with

the industry standard PCI Local Bus Specification.” *EMC II*, 2022 WL 1562847, at \*1; *see also EMC I*, 2021 WL 1088207, at \*2. ACQIS’ attempts to re-litigate the PCI claim construction should be rejected.

### **3. Plaintiff’s Proposal of “Backwards Compatibility” is Contrary to the Intrinsic Record.**

ACQIS’ proposal of “backwards compatibility” seeks, in effect, to eliminate the required “PCI Bus transaction.” The plain language of the claims require a “PCI Bus transaction.” ACQIS attempts, nonetheless, to broaden this term, by adding “backwards compatibility” to capture entirely serial PCIe transactions, with no relation to the PCI Local Bus Specification. ACQIS is incorrect. “An ‘analysis’ that adds words to the claim language without support in the intrinsic evidence in order to support a claim of infringement does not follow standard canons of claim construction.” *Source Vagabond Sys. Ltd. v. Hydrapak, Inc.*, 753 F.3d 1291, 1299–1300 (Fed. Cir. 2014). Here, the specification emphasizes use of and compliance with the PCI Local Bus Specification. Indeed, the patents incorporate the PCI Local Bus Standard as prior art. *See, e.g.*, ’750 patent, p. 6 (listing as prior art PCI Local Bus, “PCI Local Bus Specification,” and “Dec. 18, 1998, Revision 2.2”); ’769 patent, p. 6 (same). “[P]rior art cited in a patent or cited in the prosecution history of the patent constitutes intrinsic evidence.” *Kumar v. Ovonic Battery Co.*, 351 F.3d 1364, 1368 (Fed. Cir. 2003).

Further, the specification identifies the “present invention” as using and complying with the PCI Local Bus Specification. *See, e.g.*, ’797 Patent, 5:33–41 (explaining that the “present invention overcomes the . . . disadvantages of the prior art by interfacing two PCI or PCI-like buses using a non-PCI or non-PCI-like channel,” and that in the “present invention, PCI control signals are encoded into controls bits” and then, “at the receiving end” are “decoded back into PCI control signals prior to being transmitted to the intended PCI bus”); *id.* at Fig. 16, 8:35–37 (listing the “names, types, number of pins dedicated to, and the description of the primary PCI bus signals”); *id.* at Fig. 13, 21:1–8 (discussing the invention’s use of “PCI control signals,



such as FRAME#, IRDY#, and TRDY#”), 17:29–62 (describing parallel to serial conversion for conducting PCI transactions, using the same components of parallel transactions, encoded and translated for serial data transmission). Where “a patentee describes the features of the ‘present invention’ as a whole, he implicitly alerts the reader that this description limits the scope of the invention.” *Luminara Worldwide, LLC v. Liown Elecs. Co.*, 814 F.3d 1343, 1353 (Fed. Cir. 2016) (internal quotation marks omitted). This makes sense, as a claim term is understood to have its plain meaning “at the time of invention”—then, as now, “PCI” means the PCI Local Bus Specification. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (*en banc*); *see generally* Ex. A, PCI Local Bus Specification Rev. 2.2.

What is more, ACQIS itself has strenuously argued for the construction the Federal Circuit adopted, expressly disclaiming non-PCI transactions to preserve validity. In IPRs, ACQIS distinguished prior art for not including a full PCI bus transaction with all address, data, and control bits. Referring to the address, data, and control bits of a PCI bus transaction, ACQIS’ counsel emphasized: “[Y]ou got to have them all because you are going by the PCI standard.” Ex. C, *EMC*, IPR2014-01462, Paper 60 at 49:12–16; *see also, e.g., id.* at 35:13–17, 38:9–17 (ACQIS stating that the claims require “the information necessary to make a PCI transaction under the defined standard,” which “includes the control bits every time”), 49:24–50:2 (distinguishing prior art as not “*interested in speeding up a PCI standard transaction*”) (emphasis added); Ex. D, *EMC Corp. v. ACQIS LLC*, IPR2014-01462, Aug. 27–28, 2015 Dep. Tr. of Volker Lindenstruth Vols. I and II, at 145:18–146:17, 154:4–8 (PTAB Sept. 10, 2015) (ACQIS’ expert stating “a PCI bus transaction . . . has to include everything”). In regard to IPR claim construction, ACQIS expressly said:

The proper construction for “Peripheral Component Interconnect (PCI) bus transaction” is . . . “Peripheral Component Interconnect (PCI) industry standard bus transaction.” Any other reading of the term would render the phrase “PCI” meaningless. . . . The PCI industry standard was well known at the time of the invention, and [a POSITA] would not confuse the PCI transaction for any other transaction.



Ex. B, *EMC*, IPR2014-01462, Paper 30 at 17–18. As ACQIS explained, “adherence to the [PCI Local Bus Specification] is critical for interoperability,” because “[e]ven minor deviations from a standard will result in incompatible hardware and software.” *Id.* at 8. These statements made by the patentee during an IPR constitute intrinsic evidence. They are also clear disclaimer. *See Aylus Networks, Inc. v. Apple Inc.*, 856 F.3d 1353, 1361 (Fed. Cir. 2017) (“Because an IPR proceeding involves reexamination of an earlier administrative grant of a patent, it follows that statements made by a patent owner during an IPR proceeding can be considered during claim construction and relied upon to support a finding of prosecution disclaimer.”). A “patent may not, like a nose of wax, be twisted one way to avoid anticipation and another to find infringement.” *CommScope Techs. LLC v. Dali Wireless Inc.*, 10 F.4th 1289, 1299 (Fed. Cir. 2021).

#### **4. Plaintiff’s Proposal of “Backwards Compatibility” Creates Ambiguity and Invites Jury Confusion.**

ACQIS proffers, but fails to define, what “backwards compatibility” means, or what the scope of those two words might be. What is clear is that, at the time of invention, the PCI Local Bus Specification was well-known, as was the meaning of PCI transaction, and that the inventor relied on that knowledge and meaning in drafting the Asserted Patents. *See* Ex. A, PCI Local Bus Specification Rev. 2.2 at 1 (PCI was “developed in 1992,” “successfully met [the] demands of the industry and is now the most widely accepted and implemented expansion standard in the world”); *see also, e.g.*, ’797 patent, 7:37–40. Adoption of all PCI Local Bus Specification requirements allowed for standardization and interoperability, which the inventor emphasized. Ex. B, *EMC*, IPR2014-01462, Paper 30 at 3.

The Asserted Patents lack any disclosure on compatibility in the absence of a complete PCI transaction. Whatever the precise contours of the phrase, if the claims encompass “backwards compatibility,” they lack written description and enablement support. “[T]he specification must enable the full scope of the invention as defined by its claims.” *Amgen Inc.*

*v. Sanofi*, 598 U.S. 594, 610 (2023) (“The more one claims, the more one must enable.”); *see also Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (*en banc*) (invalidating claims for lack of written description, because “the specification must describe an invention understandable to that skilled artisan and show that the inventor actually invented the invention claimed”).

What is clear is that ACQIS once again seeks to extend its patents to PCIe, despite the Federal Circuit having already affirmed that PCIe does not practice the claimed “PCI transaction” limitations. *Compare* Ex. K, *ACQIS LLC v. Hon Hai Precision Indus. Co.*, No. 6:23-cv-264-ADA, ACQIS’ Amended Prelim. Infringement Contentions at 5 (Jan. 26, 2024) (accusing Hon Hai products “that incorporate PCI Express”), *with EMC II*, 2022 WL 1562847 at \*1, *and EMC I*, 2021 WL 1088207 at \*5–6. “PCI Express is a serial, point-to-point interface,” in contrast to PCI’s “parallel, multi-drop interface,” with “many of the rules and interactions in PCI . . . no longer directly applicable to PCI Express.” Ex. F, Adam Wilen *et al.*, *Introduction to PCI Express: A Hardware and Software Developer’s Guide* at 79 (Intel Press 2003). For example, “[t]he signaling scheme for PCI Express is tremendously simple,” with “no separate address and data signals” and “no control signals like the FRAME#, IRDY# or PME# signals.” *Id.* at 81; *see also* Ex. J, *ACQIS, LLC v. EMC Corp.*, No. 21-1772, Dkt. No. 30 (Corrected Resp. Brief) at 10–11 (Fed. Cir. Nov. 19, 2021). ACQIS cannot use “backwards compatibility” as an end-run around the Federal Circuit’s claim construction and the unambiguous intrinsic record.

## B. “USB” or “Universal Serial Bus”

| Claim Term  | Defendant’s Construction   | Plaintiff’s Construction                                  |
|---|--|---|
| “Universal Serial Bus”/<br>“USB”<br><br>'140 patent, cls. 15, 18, 20,<br>22, 23, 26, 29, 34, 36, 37<br>'654 patent, cls. 20, 23<br>'750 patent, cl. 50<br>'797 patent, cls. 30, 33<br>'769 patent, cl. 19 | “In accordance with the<br>protocols defined in the<br>Universal Serial Bus<br>Specification Revision 2.0<br>and the prior versions of this<br>standard” | No construction necessary.<br>Plain and ordinary meaning. |

The Court should adopt Hon Hai’s proposed construction because it articulates the term’s plain and ordinary meaning *at the time of invention*. ACQIS’ proposed construction serves only to obfuscate the meaning of the Asserted Patents.

### 1. At the Time of the Invention “USB” Meant USB 2.0 or Earlier.

“[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a [POSITA] *at the time of the invention*, *i.e.*, as of the effective filing date of the patent application.” *Phillips*, 415 F.3d at 1313 (emphasis added). Here, that means “USB” refers to USB 2.0, or earlier.

The date of the earliest provisional application in ACQIS’ claimed priority chain for all Asserted Patents is May 14, 1999.<sup>4</sup> Around that time, the latest version of the USB Specification in existence was Revision 2.0 (the “USB 2.0 Specification”). *See* Ex. G, USB 2.0 Specification at 1 (Apr. 27, 2000). The non-reissue patents confirm this by explicitly reciting the use of USB 2.0. *See, e.g.*, ’797 patent, 11:49–50 (“For example, the invention can use Gbit Ethernet 1394, and USB 2.0.”), 11:61–63 (“The implementation . . . can use other high-speed serial communication such as USB 2.0”). Further, the Asserted Patents specifically

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<sup>4</sup> For the first time in this case, after a decade of related litigation, ACQIS has attempted to claim January 1998 as the time of the invention. Ex. K, *ACQIS LLC v. Hon Hai Precision Indus. Co.*, No. 6:23-cv-264-ADA, ACQIS’ Amended Prelim. Infringement Contentions at 1–2 (Jan. 26, 2024). An earlier date only further strengthens the argument against ACQIS’ capture of later-invented technology through an ambiguous claim construction.

limit the “present invention” to “implement[ation] using conventional technologies”—*i.e.*, those in existence at the time of the invention. *Id.* at 7:37–40; *see also Luminara*, 814 F.3d at 1353 (“When a patentee describes the features of the ‘present invention’ as a whole, he implicitly alerts the reader that this description limits the scope of the invention.”). Because the ordinary meaning of a term is “defined by what was known in the art at the time,” a POSITA would understand the patent’s references to “USB” to mean to USB 2.0, or earlier. *Massachusetts Inst. of Tech. & Elecs. for Imaging, Inc. v. Abacus Software*, 462 F.3d 1344, 1353 (Fed. Cir. 2006); *see also, e.g., Fundamental Innovation Sys. Int’l LLC v. Samsung Elecs. Co.*, No. 17-cv-145-JRG, 2018 WL 647734, at \*11 (E.D. Tex. Jan. 31, 2018) (“[T]he term **‘USB’ in the patents-in-suit should be limited to the Universal Serial Bus standards that existed at the time of the claimed invention.**”) (emphasis added).

ACQIS has conceded as much in prior litigations, stipulating that the “the term ‘USB’” in the Asserted Patents “refers to the versions of the USB specification in existence at the time of the invention, including USB 2.0 and prior versions.” Ex. H, *ACQIS LLC v. Samsung Electronics Co., Ltd.*, No. 20-cv-295, Dkt. No. 71 at 10 (E.D. Tex. Aug. 3, 2021); *see also* Ex. I, *ACQIS LLC v. Samsung Electronics Co., Ltd.*, No. 20-cv-295-JRG, Dep. Tr. of Marc E. Levitt at 43:5–18 (E.D. Tex. June 23, 2021) (“[W]ithin the patents and what is mentioned in the time frame, it is—it would be the appropriate parts of USB 2.0 or potentially earlier versions, which would be 1.1.”). ACQIS cannot now credibly extend its claims to the much later USB 3.0. specification. “A claim cannot have different meanings at different times; its meaning must be interpreted as of its effective filing date.” *PC Connector Sols. LLC v. SmartDisk Corp.*, 406 F.3d 1359, 1363 (Fed. Cir. 2005).

## **2. Plaintiff’s “Plain and Ordinary Meaning” Invites Jury Confusion.**

Plaintiff urges the Court to adopt a bald “plain and ordinary” meaning. Arguing “plain and ordinary meaning,” however, does not obviate a party’s obligation to say what that plain

and ordinary meaning is, so that the Court can make a determination as to the disputed claim scope. *O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co., Ltd.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008); *see also, e.g., SitePro, Inc. v. Waterbridge Resources LLC*, No. 23-cv-115-ADA-DTG, 2024 WL 760923, at \*3 (W.D. Tex. Feb. 23, 2024) (where parties dispute a term's scope "the Court must describe what the plain-and-ordinary meaning is").

Here, ACQIS attempts to use "plain and ordinary meaning" to capture technology the inventor did not, and could not have, foreseen, much less invented. Nothing in the Asserted Patents supports broadening the term "USB" beyond what a POSITA would have understood at the time of invention. Rather, the claims recite use of standard USB "protocol data," with the specification emphasizing that the "present invention is . . . implemented using conventional technology." '797 patent, 7:37-40; *see also, e.g., id.* at 41:31 ("conveying Universal Serial Bus (USB) protocol data"). At the time of invention, a USB "protocol" was a "specific set of rules, procedures, or conventions relating to format and timing of data transmission between two devices." Ex. G, USB 2.0 Specification at 8.

Under the USB 2.0 Specification, the recited "protocol / data information" requires an 8-bit packet identifier (PID), a data field containing zero or more bytes of data, and a 16-bit cyclic redundancy (CRC) value. *Id.* at 206, Figs. 8–15; *see also id.* at 18–19 (USB 2.0 transactions require three elements: a "token packet," a "handshake packet," and a "data packet"). These specific rules allowed for standardization and interoperability, and the purported inventor here relied on that standardization and conventionality. The Asserted Patents teach nothing more or different from the details set forth in the USB 2.0 Specification. Indeed, the Asserted Patents lack sufficient written description or enablement to extend the invention beyond the USB technology that was "conventional" at the time of invention, as the "hallmark of written description is disclosure." *Ariad Pharms.*, 598 F.3d at 1351; *see Amgen*, 598 U.S. at 610. The Asserted Patents have no disclosure whatsoever as to USB 3.0—

nonetheless, as with PCIe, ACQIS attempts to extend its patents to USB 3.0. Ex. K, *ACQIS LLC v. Hon Hai Precision Indus. Co.*, No. 6:23-cv-264-ADA, ACQIS’ Amended Prelim. Infringement Contentions at 5 (Jan. 26, 2024).

Where, as here, “a claim term understood to have a narrow meaning when the application is filed later acquires a broader definition, the literal scope of the term is limited to what it was understood to mean at the time of filing.” *Kopykake Enterprises, Inc. v. Lucks Co.*, 264 F.3d 1377, 1383 (Fed. Cir. 2001); *see also Extreme Networks, Inc. v. Enterasys Networks, Inc.*, No. 07-cv-229, 2007 WL 5601497, at \*17 (W.D. Wis. Nov. 21, 2007) (declining to “expand[] the reach of a claim beyond what could have been anticipated by the inventor”). Plaintiff’s attempt to broaden the meaning of USB, through a vague construction, would only serve to confuse the jury and capture subject matter neither contemplated by the inventor nor supported by the specification.

#### **IV. CONCLUSION**

Hon Hai respectfully requests that the Court adopt its proposed claim constructions.

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Respectfully submitted,

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**CERTIFICATE OF SERVICE**

I hereby certify that on March 14, 2024, all counsel of record were served with the foregoing document via electronic service.

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